An implantable 700µW 64-channel neuromodulation IC for simultaneous recording and stimulation with rapid artifact recovery

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Abstract

We present an 180nm HV CMOS IC for concurrent neural stimulation and recording that combines 64 low-noise recording front-ends and 4 independent stimulators multiplexed to any of the 64 channels. The stimulators have 5mA peak current, 12V compliance and dynamic power management to maximize efficiency. Co-design of the stimulation and recording subsystems resulted in 100mV of recording linear range, 70nV/rtHz noise, and a rapid 1ms (single-sample) artifact recovery during stimulation.

Keywords: artifact, neural, recording, stimulation

Introduction

Neurostimulation (NS) has seen widespread adoption in the treatment of movement disorders, pain, and epilepsy, and has shown promise in treating psychiatric disorders, memory loss, depression, and more [1]. A state-of-the-art NS device applies periodic zero-mean current pulses to the brain, with parameters determined heuristically by a clinician. Threshold currents for typical NS targets can be mAs through electrodes with several kΩs of series resistance, necessitating a stimulation compliance ≥10V. Recently, NS devices have added the ability to record neurological signals and stimulate in response to specific biomarkers *in situ*, reducing power. Concurrent sensing and stimulation remains a great challenge in realizing true closed-loop operation [1] since stimulation can saturate amplifiers and create large, long-lasting artifacts that corrupt the signal. Most systems must stimulate and record at different times or in separate brain regions. To enable true closed-loop operation, the recording and stimulation subsystems must be co-designed to minimize interference and rapidly recover from stimulation artifacts as high as ~100mV.

System Description and Measurements

The neuromodulation IC (NMIC) shown in Fig. 1 enables simultaneous 64-channel neural recording and stimulation, and meets all the requirements described above. The NMIC features 64 low-noise and high dynamic range neural recording front-ends and 4 high-compliance stimulators with rapidly reconfigurable locations (any of 64 electrodes), amplitudes, pulse timing, and frequencies. Stimulation and recording hardware are reused to perform impedance measurement on all electrodes. It incorporates a 6-wire power and data transfer architecture, simplifying cabling. A 2Mbps bidirectional data interface enables constant recording, rapid reprogramming, and system monitoring to ensure safe operation. Power and clock are derived from a 20MHz, 3VAC input voltage and rectified to a 3VDC supply voltage, or supplied from a 3V battery. Programmable DC-DC converters with >80% measured power efficiency provide a 1V supply to the recording and digital subsystems as well as a 3/6/9/12V supply to the stimulator, adjusting the compliance for different stimulation regimes to increase efficiency.

Recording and stimulation compatibility is achieved through common referencing at ground, charge balancing of the stimulation, and a front-end with rapid overload recovery and a large linear input range. The recording subsystem (Fig. 2) is

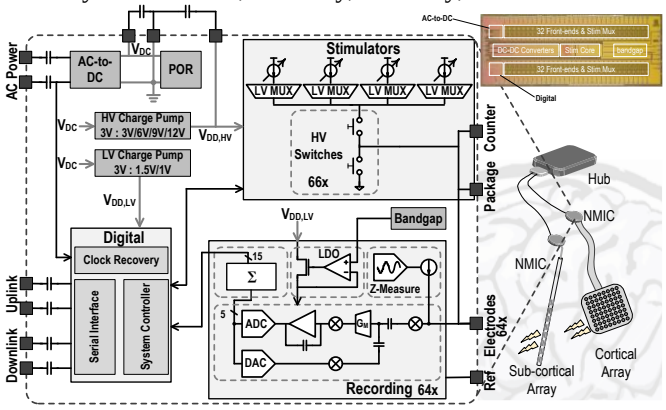

Fig. 1: System diagram and concept illustration of the NMIC.

comprised of 64 mixed-signal 1kS/s 15-bit front-ends. Each front-end has a separate LDO to minimize power supply coupling. The front-ends have a programmable full-scale input voltage (V_{fsDAC}) of ±50mV - ±200mV allowing simultaneous amplification and digitization of the electrode offset, neural signal, and stimulation artifact within the linear range. A higher linear input range than state of the art [2-5] is achieved by bringing the ADC inside the capacitive feedback loop, reducing the needed signal swing at internal nodes. Low noise is achieved through chopper-stabilization of the Gm stage and a current-input loop filter that suppresses noise at harmonics of the sample rate. A 5-bit, 1024x-oversampled SAR ADC results in a 15-bit output and a charge-redistribution DAC provides feedback at the Gm input, creating a virtual ground. The front-end gain is $C_{AC}/(C_{DAC}V_{fsDAC})$, independent of temperature and manufacturing variations. S_{RST} switches are closed during a brief reset phase to store the offset of the Gm on C_{AC}, minimizing chopper ripple and aiding in rapid recovery by clearing the memory of the previous sample. The sampled kT/C_{AC} noise is converted into out-of-band chopper ripple, enabling small values of C_{AC} and high input impedance since $Z_{in}=1/(4C_{AC}f_{CHOP})$. The measured front-end linear input range is ~100x greater than state-of-the-art [2-5] with 55dB higher dynamic range, lower THD, 1.8x lower VDD, and lowest PEF.

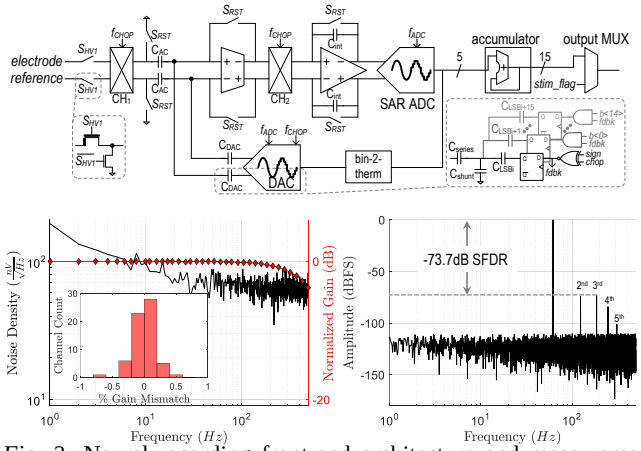

Fig. 2: Neural recording front-end architecture and measurement results. Noise spectrum is input-referred and SFDR spectrum is normalized to full scale input.

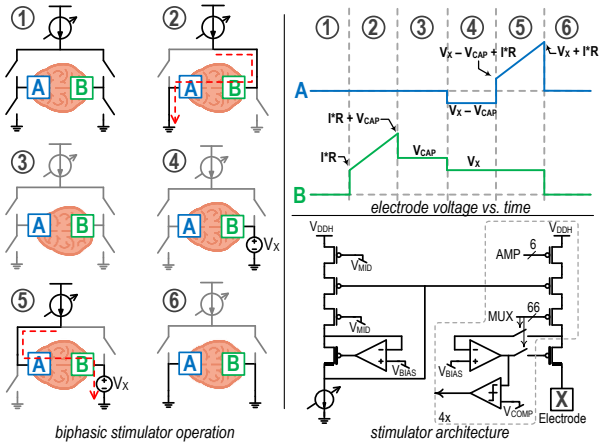

Fig. 3: Principle of stimulator operation and timing diagram for an individual stimulator for a Randles circuit electrode model.

The high peak currents of the stimulators and the need for rapid artifact recovery necessitate precise current matching between phases. The stimulator architecture shown in Fig. 3 reuses the same current source for the cathodic and anodic stimulation phases to minimize charge error. Previous implementations required the stimulator electrodes to be referenced at a large VREF or VDD [4], making it difficult to combine with low-voltage recording circuits. To maximize compliance and compatibility with recording, a ground-referenced architecture is proposed. The need for a negative supply is eliminated by adding a DC offset generated by an adjustable diode string (V_X) in the 2nd phase to prevent a negative voltage at the beginning of the anodic phase resulting in a measured 0.016% mismatch for low compliance, and <1% mismatch for high compliance stimulation. A programmable passive recharge phase further reduces residual charge and DC offsets on the electrodes. The stimulator can produce monophasic, biphasic, and other arbitrary waveforms, can store patterns and be reprogrammed up to every 4ms for closed-loop applications. Multiple stimulators can be combined on a single electrode to produce complex waveforms (Fig. 4) or high currents up to 20mA.

In vivo Validation

The NMIC was assembled with a Pt-Ir and W electrode microdrive and implanted in the motor cortex of an adult macaque monkey (Fig. 5). Recordings were taken during a motor task with a juice reward upon task completion. Readout on all channels was performed and shows β-band (13-30Hz) power decrease during movement and increase during a hold period and reward, consistent with neuroscientific results. Simultaneous biphasic stimulation (15Hz, 150µA) and recording in the motor cortex resulted in a 1ms (single-sample) stimulation artifact. Multi-channel PCA denoising was used to remove the stimulation artifact and recover the underlying

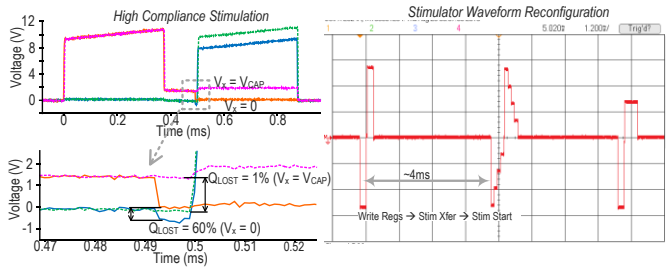

Fig. 4: Stimulation waveforms demonstrating rapid reconfiguration of arbitrary stimulation waveforms and high compliance stimulation.

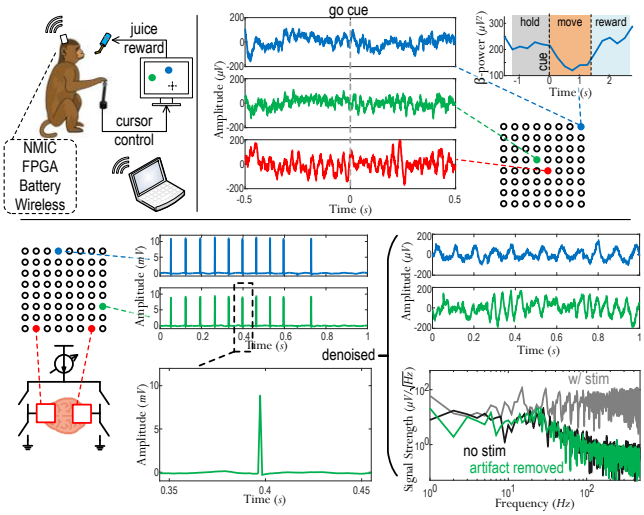

Fig. 5: Illustration of the experimental setup and spectrum recovery from ~8mV stimulation artifact.

biological signal spectrum. All *in vivo* experiments were performed in compliance with the NIH Guide for the Care and Use of Laboratory Animals.

Conclusion

The IC is fabricated in an 180nm 1P6M HV CMOS process and occupies 11.52mm^2. The total power dissipation of the chip is stimulation protocol dependent, and is 700µW in typical configuration, including power management circuits. We compare against recently published bidirectional neural interface ICs in Table 1. The NMIC integrates the highest degree of stimulator programmability and highest peak current with the highest dynamic range recording, while achieving state-of-the-art noise and power performance. Co-design of the recording and stimulation subsystems enables saturation-free recording during stimulation with a 1ms (single sample) artifact, and with the potential to enable true closed-loop neuromodulation.

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References

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Table I. Summary and Comparison

		[3]	[4]	[5]	THIS WORK
SYSTEM	Recording Channels	4	256	16	**64**
	Stim. Channels/No. of Stimulators	2 + 8 / 2 + 8[a]	64 / 64	160 / 40	**64 / 4**
	Impedance Meas. Channels	0	0	48	**64**
	Data Rate Tx / Rx (Mbps)	0.8 / 0.1 (RF)	20 / -- (Wireline)	2 / 2 (RF)	**2 / 2 (Wireline)**
	Power Supply	915 MHz RF or 5V Battery	$3V_{DC}$	2 MHz RF	**$3V_{AD}$, 20MHz or 3V Battery**
	Technology (nm)	180	350	180 HV	**180 HV**
	Die Size (mm^2)	4	12.8	25.1	**11.52**
	Tot. Power Dissipation (mW)	0.47	13.5	--	**0.7**
RECORDING	Power/Channel (µW)	61.2	52	5.4	**8**
	Supply Voltage (V)	1.8	3.3	±1.8	**1**
	Input-Referred Noise (nV/rtHz)	81	82	92	**71**
	NEF / PEF	9.3 / 157	8.9 / 261	6.2 / 138	**7.8 / 60.8[b]**
	ADC Res. / ENOB (bits)	8 / 5.6	8 / 5.1	-- / 8.5	**15 / 10.2**
	Input Range (mVptp)	1.2	1	--	**100 / 400[c]**
	Dynamic Range (dB)	35.5	32.9	--	**90**
	THD	1.7% (1.2mVptp)	0.8% (1mVptp)	--	**0.7% (100mVptp)**
STIMULATION	Max Current (mA)	4.2 / 0.12 (6 bit)	0.25 (--)	0.5 (7 bit)	**5.04 (8 bit)[d]**
	Supply Voltage (V)	5	3.3	±6/±12	**3/6/9/12**
	Frequency (Hz)	15.4	--	Up to 20k	**15 – 255 (8 bit)**
	Pulse Width (us)	1000	150 – 230	10 - 800	**15 – 500 (6 bit)**
	Charge Cancellation	No	No	Yes	**Yes**
	Stimulation Recovery Time	Not simultaneous	N/A	Distant	**1ms**
	Type	Biphasic	Mono&Biphasic	Biphasic only	**Mono&Biphasic**

[a]2 high-current stimulators and 8 low-current stimulators
[b]**includes ADC**
[c]Input range expandable to 400mVptp
[d]All 4 stimulators can be combined for total Istim = 20.16mA